HDC-2900

HARD DISK CONTROLLER

TECHNICAL MANUAL

Systems Group

A Division of MEASUREMENT systems & controls incorporated

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1.0 General Description

The HDC-2900 Hard Disk Controller board is a unique product which was designed to control SA-4000 interface Winchester Hard Disks. The addition of different personality boards allows the controller to talk to other types of disk interfaces (SA-1000, ST-506, ANSI, and SMD) at the same time. This flexibility allows the user to update his disk capabilities at a later date. The HDC-2900 also allows the use of two sector sizes (256 or 512 bytes per sector). The HDC-2900 occupies four I/O address spaces leaving maximum memory space available to the user.

2.0 Specifications

Bus Interface	Proposed IEEE S-100 (696)
Hard Disk Interface	SA-4000 type interface
Number of Hard Disks Supported (without personality boards)	2
Sector Buffer Size	1024x8 bits
Interrupts	two software maskable interrupts strappable to VI0 thru VI7
Sector Buffer Access	Data goes through a single I/O address
Sector ID Overhead	Four Bytes
Software	Software Compatible with HDC-2800 drivers
Expansion Capabilities	ST-506, SA-1000, ANSI, and SMD interfaces (Expanded through the use of Personality boards).
Maximum Data Rate	10 Megabits per second
Power Requirements (without personality boards)	+8 volts at 1.6 amps max.
Temperature	0 to 45 degrees Celsius
Relative Humidity	0 to 95% relative humidity non-condensating
Shock	Five G/10 millisecond shock
Vibration	2 to 50 Hertz, one inch double amplitude
Testing	Fully tested and burned-in

3.0 HDC-2900 Strapping Options

The following section describes the strapping options of the HDC-2900 Hard Disk Controller board.

3.1 Board I/O Address Strapping

The HDC-2900 is caple of being addressed at on any one of 64 locations in the I/O area. Jumpers E2 through E7 set the base address of the board. The board is usually set to a base address of 0C0 hex when used with Systems Group Software. Each E jumper represents an address bit on the S-100 bus. The address bit to E jumper coorelation is as follows:

Address Bit	Jumper
AD7	E7
AD6	E6
AD5	E5
AD4	E4
AD3	E3
AD2	E2

The addresses match when all the states of the E jumpers match the addresses coming in on the S-100 bus. Jumpering an E point means that when the address bit cooresponding to that jumper is an electrical low (less than .8 volts) for a match. For example; to jumper a HDC-2900 for a base I/O address of 0C0 hex, jumpers would be on E2, E3, E4, and E5.

3.2 Interrupt Strapping

The HDC-2900 has two software maskable interrupt sources. The seek complete and the operation done interrupts are maskable by setting bits in the control port (see section on software considerations). The seek complete interrupt may be strapped to vectored interrupt lines VI0, VI2, VI4 or VI6 on the S-100 bus. The operation done interrupt may be strapped to vectored interrupt lines VI1, VI3, VI5 or VI7. Systems Group software expects VI2 and VI3 to be strapped with the exception of OASIS systems which do not use interrupts.

Typical Drive Strapping

Switch # 3

Position	On/Off	
1	On	
2	On	
3	Off	
4	Off	
5	Off	DS3
6	Off	DS2
7	Off	DS1
8	On	DS0

Switch # 4

Position	On/Off
1	Off
2	Off
3	Off
4	Off
5	Off
6	Off
7	Off
8	Off

Switch # 5

Position	On/Off
1	On
2	On
3	On
4	Off

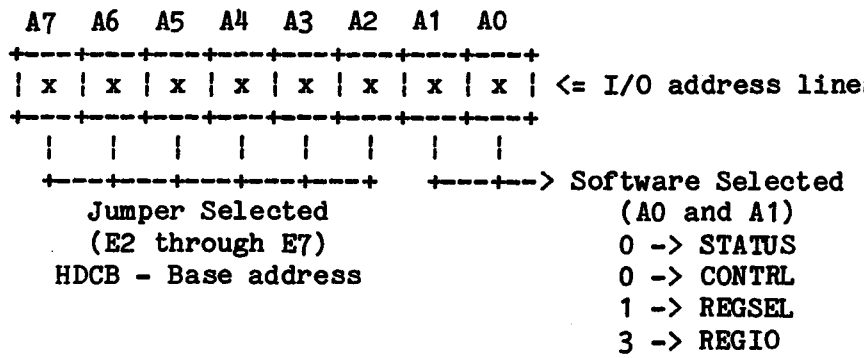
Jumper "S1" pins 1-2 for -5vdc supply.

5.0 SOFTWARE CONSIDERATIONS

This section breifly covers the programming of the HDC-2900. Detailing the I/O port definitions and provides an overall view of how the controller performs its functions. Examples of software drivers written in Z-80 code are at the end of this section.

5.1 I/O Port Addresses.

The HDC-2900 occupies 4 contiguous I/O port addresses that may begin on one of 64 boundries. The following figure designates which I/O address lines are hardware or software selected:



5.2 The Status Port Definition (STATUS, HDCB+0).

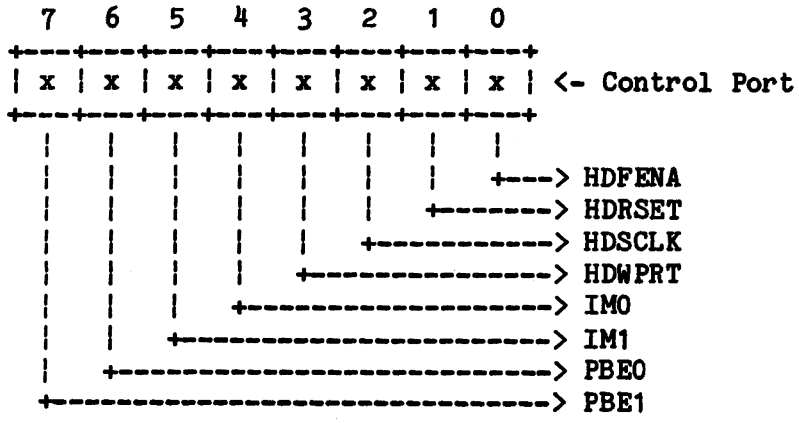
This port is Read Only and contains status on the condition of the on board state machine as well as the condition of the disk interface bus. The bits are defined as follows:

each time an index pulse is detected on the disk interface bus. It is used as a rotational signaling bit if revolutions of the disk need to be detected.

HDNBSY - Hard disk controller not busy. This bit goes high (1) when the controller's on-board state machine is ready to accept an input/output command to registers or ports other than the main status port (STATUS) or the control port (CONTRL). This bit should be tested before any other board operation.

5.3 The Control Port Definition (CONTRL, HDCB+0).

The control port is Write Only and gives the programmer control over the current state of the controller. Although this port is latched on the controller board, it cannot be read, requiring an image to be maintained of this port in the software. The port contains the following control bits:

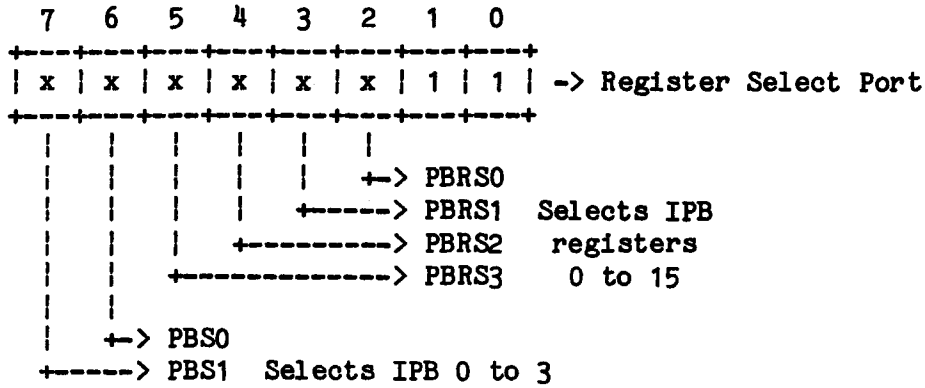


HDFENA - Hard disk function enable. This bit must be set high (1) for the controller to latch in changes to the function register (FUNTCN). When this bit is low (0), all writes to the function register are ignored.

HDRSET - Hard disk reset. This bit is set high for normal operation of the controller. Strobing this bit first low (0), then high (1) performs a hardware reset of the board, much the same as the external reset line on the S100 bus.

HDSCLK - Hard disk controller clock select. This bit is set low for the controller to operate from the S100 clock input or set high for the controller to operate from the disk interface bus clock. Because the clock on the disk interface bus is multiplexed, it is available only if a drive is selected and ready for operation. Data operations are performed best when the controller is operating from the disk interface bus clock. Therefore the controller should only be switched to the disk interface bus clock just prior to a read or write operation, and only if

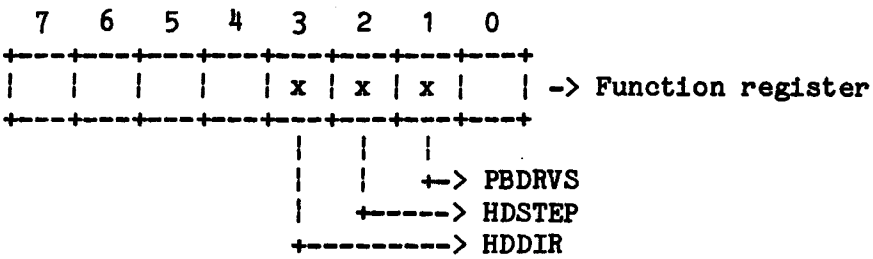
When HDC registers are selected, bits 2 through 7 have no meaning. When IPLSEL condition is selected (bits 2 through 7 are defined as follows:



The paddle board select bits (PBS0, PBS1) select one of the four possible IPB's connected to the controller, while the paddle board register select bits (PBRS0 - PBRS3) select one of the sixteen possible registers on each possible IPB. This allows the selection of up to 64 offboard registers.

5.4.1 FUNCTN - Function register.

This register is write only and gives the programming controll over drive selection and drive interface step functions. Two drives attached to the HDC-2900 locally or eight (8) drives attached to IPB's externally may be selected through this port. For drives attached to the HDC-2900 only, this register contains four (4) bits for head selecting. The layout of the register is as follows:

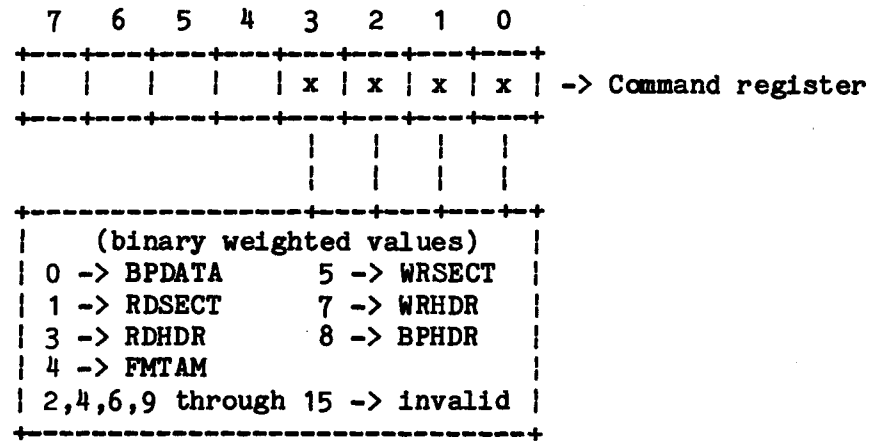


PBDRVS - Paddle board drive select. When this bit is set high (1), drive and head select operations are performed through an IPB register (see below). Drives connected to IPB's are usually not SA-4000 type drives. When this bit is set low (0), SA-4000 type drive and head select operations are performed through this register as follows:

IPBA - Interface personallity board acknowledge. This bit goes high (0) if the selected IPB is connected to the controller, otherwise it remains low (1). This bit is useful for determining whether a particular type drive may be supported by the controller.

5.4.4 COMMD - Controller command register.

This write only register holds the current command for the controller to perform. Before this register may be written, the HDNBSY bit in the main status port (STATUS) must be high (1). Valid commands to the register are as follows:



BPDATA - Buffer pointer to data area. This command sets the on-board buffer pointer to the data area. Data transfered though the data register will begin at this buffer. See the note below.

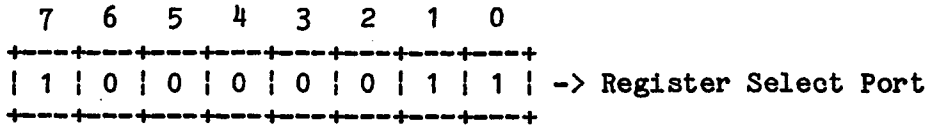
RDSECT - Read a sector. This command instructs the controller to read the sector currently described in it's header buffer. The header buffer must be setup before this command is issued. The HDCCMP bit in the main status port (STATUS) will be set high (1) after the completion of this command. Further bits are tested in the STATUS port and STATB register to determine the success of the read a sector command.

RDHDR - Read a header. This command instructs the controller to read the header from the next encountered ID field on the disk. The HDCCMP bit in the main status port (STATUS) will be set high (1) after the completion of this command. If 16 revolutions of the disk occur and a valid ID field has not been found, the controller terminates the command and sets the HDTOUT bit in the main status port.

FMTAM - Format Address Marks. This is a special command that instructs the controller to write continuous blank data onto the disk. It is only used with ST-506 and SA-1000 type drives which use address marks on the disk to determine sector boundries. In formatting these types of drives,

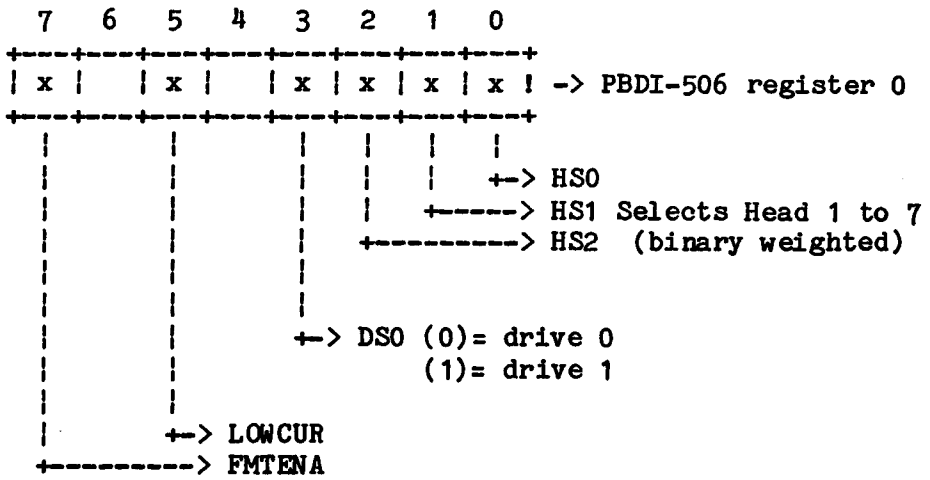
5.5 The ST506 Interface Personallity Borad (PBDI-506).

This IPB allows the use of hard disk drives with the ST506 type of interface. Currently only one (1) register is defined for this IPB. To select the register on this IPB through the controller, use the following values for the two personallity board select lines.



If this IPB is presently attached to the controller, the IPBACK bit in the STATB register go high (1) after the selection.

The one register located on the BPDI-506 is defined as follows:



LOWCUR - Low current enable. This bit set high (1) to enable the low current write logic on the BPDI-506 interface board. When Drives requiring low current writes are used, this bit must be high on all cylinders requiring low current writes.

FMTENA - Format drive enable. This bit is normally set to the low (0) state, but just prior to the write header command, must be set high (1), and one complete revolution of the disk must occure. FMTENA functionally switches the detection of ID address marks from the hard disk (normal operation) to counter derived marks so that the formatting of headers may be performed.

revolutions of the disk occure and the controller cannot match the header on the disk with the header in the buffer, then the HDTOUT and HDCCMP bit are both set in STATUS. The HDCRC bit in STATB will also be set if a CRC error was encountered in reading the ID field. No data will be transfered unless a header match occures without a CRC error.

5.7.1 Board Initialization.

The following routine is an example of initializing the HDC-2900.

```
LD      A,(CLIMG)       ; image of control port
RES     HDRSET,A        ; lower reset line
OUT     (CONTRL),A      ; send it to reset
SET     HDRSET,A        ; raise reset line
OUT     (CONTRL),A      ; send again to clear
CALL    WTNBSY          ; test controller busy
LD      A,(RSIMG)       ; image of reg sel port
OR      FUNCTN          ; set function reg select
OUT     (REGSEL),A      ; send select code
LD      A,(FLIMG)       ; image of function reg
OUT     (REGIO),A       ; and send to reg
```

5.7.2 Command output.

The following subroutine shows how the controller should be tested before an operation is sent to the command register (COMMD). The command is assumed to be in the A register.

```
CMDOUT:
        PUSH    AF              ; save command
        CALL    WTNBSY          ; test controller busy
        LD      A,(RSIMG)       ; image of reg sel port
        OR      COMMD           ; add COMMD sel code
        OUT     (REGSEL),A      ; send it
        POP     AF              ; restore command
        OUT     (REGIO),A       ; send command register
        RET                     ; done

; The wait not busy routine will test the not busy bit in ; the main
status port and loop untill the controller is ; ready. ; WTNBSY:
        IN      A,(STATUS)      ; read main status
        BIT     HDNBSY,A        ; test not busy bit
        JR      Z,WTNBSY        ; if busy, loop
        RET                     ; done
```

```
SKWAIT:
        IN      A,(STATUS)      ; get main status
        BIT     HDSCMP,A        ; seek done?
        JR      Z,SKWAIT        ; if not, wait in loop
        RET                     ; done
```

The following subroutine waits for one complete revolution of the hard disk to issure that heads are settled after a seek type of operation.

```
SETTLE:
        LD      B,1 SHL HDINDX  ; mask for index bit
        IN      A,(STATUS)      ; get main status
        AND     B               ; mask out index
        LD      C,A             ; and save it
STL.1:  IN      A,(STATUS)      ; get status
        AND     B               ; mask out index
        CP      C               ; index detected?
        JR      Z,STL.1         ; if not, wait in loop
STL.2:  IN      A,(STATUS)      ; get status
        AND     B               ; mask out index
        CP      C               ; index detected?
        JR      NZ,STL.2        ; if not, wait in loop
        RET                     ; done
```

5.7.4 Seek Cylinder.

The following subroutine is an example of seeking to a cylinder. It is assumed that the controller is initialized, a drive has been selected and tested to be ready for operations, and has also been recalibrated to issure that the present cylinder number is known. Two subroutines from the recalibrate subroutine (SKWAIT and SETTLE) are called by this subroutine.

The new cylinder number is assumed to be in the DE register pair.

```
SEEK:
        LD      A,(CLIMG)       ; image of control port
        RES     HDSCLK,A        ; set for S100 clock
        OUT     (CONTRL),A      ; send to port
        LD      (CLIMG),A       ; restore image
        LD      HL,(PCN)        ; get present cyl number
        OR      A               ; clear CY
        SBC     HL,DE           ; HL = magnitude
        RET     Z               ; same = null seek
        LD      (PCN),DE        ; store new cyl number
        LD      A,(FLIMG)       ; image of function reg
        LD      D,A             ; store in reg
        SET     HDDIR,D         ; preset for step out
        JR      NC,SK.1         ; if stepping out
        RES     HDDIR,D         ; now set for step in
```

```
        CALL    CMDOUT          ; send to HDC
        CALL    WTNBSY          ; test controller busy
        LD      A,(RSIMG)       ; image of reg sel port
        OR      DATA            ; data reg sel code
        OUT     (REGSEL),A      ; send it
        LD      C,REGIO         ; for indirect addressing
        IN      A,(C)           ; 2 dummy reads to
        IN      A,(C)           ; sync up pointer
        LD      B,0             ; init INIR count reg
        INIR
        INIR                    ; move 512 bytes
        RET                     ; done

WRITE:
        LD      A,BPDATA        ; point data buffer command
        CALL    CMDOUT          ; send to controller
        CALL    WTNBSY          ; test controller busy
        LD      A,(RSIMG)       ; image of reg sel port
        OR      DATA            ; data reg sel code
        OUT     (REGSEL),A      ; send it
        LD      C,REGIO         ; for indirect addressing
        LD      B,0             ; init OTIR count reg
        OTIR
        OTIR                    ; move 512 bytes
        LD      A,WRSECT        ; get HDC command
        CALL    RW              ; use common code
        RET                     ; done


RW:
        PUSH    AF              ; save HDC RW command
        LD      A,BPHDR         ; point header buffer command
        CALL    CMDOUT          ; send to controller
        CALL    WTNBSY          ; test controller busy
        LD      A,(RSIMG)       ; image of reg sel port
        OR      DATA            ; data reg sel code
        OUT     (REGSEL),A      ; send it
        LD      C,REGIO         ; for indirect addressing
        LD      HL,HDRIMG       ; address of header image
        LD      B,4             ; length of header
        OTIR                    ; send to buffer
        LD      A,(CLIMG)       ; image of control latch
        SET     HDSCLK,A        ; set to use disk clock
        SET     HDWPRT,A        ; clear drive write protect
        OUT     (CONTRL),A      ; send value
        POP     AF              ; restore HDC RW command
        CALL    CMDOUT          ; and send command
RW.1:
        IN      A,(STATUS)      ; get main status
        BIT     HDCCMP,A        ; RW complete?
        JR      Z,RW.1          ; if not, wait in loop
        BIT     HDTOUT,A        ; time out error?
```

DWG. NO.	SH	REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	INITIAL RELEASE	9 22 82	
	A1	REVISED PER ECO 210	10 6 82	

J1
A7 83
A6 82
A5 29
A4 30
A3 31
A2 81

8131 U43
5VDC
RP4 4.7K SIP
E7 E6 E5 E4 E3 E2

U42 LS240
U11 LS00
U10 LS02
10 LATCH* B5

PWR A7

HALT SH2-D4 SH4-D5 SH5-C5

PAL6L8 U35
12 RDST* SH2-C4
15 WRST*
13 ADLTE* A5
14 ENABLE* SH2-B3

PDBIN 78 R10 200Ω C74?pf
SINP 46 R13 200Ω C34?pf
PWR* 77 R8 200Ω C94?pf
SOUT 45 R12 200Ω C54?pf

A0 79
A1 80

LS375 U48
D3 LATCH*

LS139 U28
5 RDATA* SH2-D7
6 RSST* SH4-D8 SH2-D6
7 RDPB* SH6-B8
12 WRDC* SH3-C2
11 WRDATA* SH4-D8
9 WRPB* SH6 B7

LS273 U44
DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0
12 SMODE SH5-C4
9 MODE B4
15 IMI SH2-B6
6 IMØ SH2-B6
16 WREN* SH3-B2
5 CNTCLK SH5-A7
19 RUN SH5-A7
16 CNTEN SH 3-D3
U21 LS240

E9 E8 E1 99 75 54
R9 200Ω
C4 47Pf
U42 LS240
U17 LS04
INIT*
INIT SH3-C6

CMDI* SH4-B6
U42 LS240
13 MODE C1

LS74 U30
S R Q̄
5VDC
CMDSTB* SH3-D6
INIT* SH3-C6 SH4-B6 SH5-B5 SH6-B7

PWR D4
ENABLL* SH2-B1 SH6-C7
DATAØ-7 SH2-C8 SH3-C8 SH4-C1 SH6-C8

LS373 U37
DO0 36
DO1 35
DO2 88
DO3 89
DO1 38
DO5 39
DO6 40
DO7 90
DATAØ DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7

LS374 U15
PAØ PA1 PA2 PA3 PBØ PB1
PBCNT SH6-B3

DØ-7 A3
A8 DØ-7
ADLTE* C4
MODE*

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±	APPROVAL	NAME	DATE
MATERIAL	DRAWN	R. Mathis	5/81
FINISH	CHECKED		
NEXT ASSY USED ON	PROJ ENGR/DSGR		
APPLICATION	MFG APPR		
DO NOT SCALE DRAWING	PROD ASSURANCE		
	PURCHASING		
	APPROVED		

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TITLE HDC-2900

SIZE D DRAWING NO 209402 REV A.1
SCALE REV IN—FILE DATE SHEET 6 OF 6

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A1-8700

DWG. NO.	SH	REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

SHI-C3 RDATA *
SH4-D8

LS244 U38

DATA7 17 DATA6 2 DATA5 15 DATA4 4 DATA3 13 DATA2 6 DATA1 11 DATAØ 8

3 D17 18 D16 5 D15 16 D14 7 D13 14 D12 9 D11 12 DIØ

DATAØ-7
SHI-A5
SH3-C8
SH4-1C
SH6-C8

SH6-C5 BDACK* 11

LS244 U36

15 RTRY 17 INTR 13

SH4-B5 SH5-B7 B6 SH4-B5

SHI-C2 RSST* 19

9 D13 5 D12 3 D11 7 DIØ

SHI-C4 SH4-D5 SH5-C5 HALT 17
SH4-D4 NRZI 2
SH3-C3 SH6-D5 RDY * 15
SH6-C5 WRERR * 4
SH3-B3 SH4-B5 TIMEOUT 13
SH5-B7 COMPLETE 6
SH4-B8 SH3-B7 B5 DONE 11
SH3-B3 SH6-D5 TKO * 8

LS244 U45

SHI-C4 RDST * 1 19

3 18 5 16 7 14 9 12

J1

D17 43 D16 93 D15 92 D14 91 D13 42 D12 41 D11 94 D10 95

SH6-B3 +8V

+5A VOUT LM340-5 VR1 VIN
C1 .1Mfd
C2 +6.8Mfd

+5B VOUT LM340-5 VR2 VIN
C8 .1Mfd
C10 6.8Mfd

J1 1 51 50 100

SHI-C1 IMI 5

LS04 U1 6 DONE 10 U2 8 38

C4 SH4-B5

SHI-C1 IMØ 9

LS04 U1 8 INTR 5 U2 6 38

D6 SH4-B5

SH5-A7 Ø2* 3 U42 17 LS240

C6 47Pf

J1 VI0 4 VI1 5 VI2 6 VI3 7 VI4 8 VI5 9 VI6 10 VI7 11

SHG-B6 +16V R11 200Ω 2 24

5VDC

4 P 74LS74 D U19 Q 2 5

10 P 74LS74 D U19 Q 12 9 ENABLL* SHI-B6 SHG-C7

SH3 C7 SH4 B8 SH5-C5,A3 CLOCK 3 11

C 1 C 13

ENABLE * SHI-C4

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

APPROVAL	NAME	DATE
DRAWN	R. Moller	5/12
CHECKED		
PROJ ENGRG/DSGN		
MFG APPD		
PROD ASSURANCE		
PURCHASING		
APPROVED		

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TITLE HDC-2900

SIZE D DRAWING NO 209402 REV A.1

SCALE REV IN—FILE DATE SHEET 2 OF 6

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A16700

DWG. NO.	SH	REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

5VDC
LS299 U31
SI 19
BYTE * 2
DATA7 16
DATA6 4
DATA5 15
DATA4 5
DATA3 14
DATA2 6
DATA1 13
DATA0 7
SH5-C5
SH5-B3,B5 SH5-D3 SH4-D8
D3 SH1-B6 SH2-C8 SH4-C1 SH6-C8
SH2-B3 SH4-B8 CLOCK SH5-A3,C5
DC2 SH5-B3 SH4-C7
9 5VDC
11 RDATA3 SH5-D1

DRDATA SH6-D2
CMDSTB* SH1-B2
INIT SH1-B6
CSO SH5-C1
CSI SH5-C1
PAL16R4 U23
4 WRGATE* B2
15 RDATA2 SH4-B8
2 CPDATA SH4-B7
18 EQUAL* SH4-D7
14 COMMAND* SH5-D5 SH4-B8,D8
CLRCRC SH4-A6
LS04 U1
9401 U14
CLOCK*

WRDATA SH6-B5
DSB SH5-B5
DCLOCK SH5-A5 SH6-C3
DSA SH5-B5
9638 U8
MC3486 U7
9638 U9
CLOCK* SH4-B4 SH5-A5
P3
P4
1000Ω R1
1000Ω R2
1000Ω R4
1000Ω R3
D8 SH1-D6 SH2-C8 SH4-C1 SH6-C8
DATA Ø-7
SH2-C4,D4 SH5-D2 SH6-C5,D5

SH2-C4 SH4-B8 COMPLETE
LS02 U10
LS04 U1
INT* SH6-C5
R5 4.7K 5VDC
R150 SIP1 RP3

SH1-B1 CNTEN
LS374 U3
DSØ SH5-B6
DSI SH5-B6 SH6-D3
DSI* SH6-A8
P1
+C4
LS240 U21
LS240 U2
DATAØ 4
DATA1 7
DATA2 3
DATA3 18
DATA4 8
DATA5 13
DATA6 14
DATA7 17
STEP*
DIR*
SH1-C2 WRDC*
SH6-B7
5VDC
INDX*
RDY*
SECTOR 14 SECTOR*
TKO* LS240
WRERR*
R150 SIP1 RP3
LS244 U36
WREN* SH1-C1
WRGATE* SH6-B7 SH5-C1
RGATE* SH5-C1 SH6-B7
FCLR*
WGATE*
RGATE*

NOTE: P2+P3 PINS 2,4,6,8,11,14,17,20 ARE GROUNDED.
P1 ODD NUMBERED PINS 1 THRU 37 AND PINS 41,47 AND 50 ARE GND.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	APPROVAL	NAME	DATE
MATERIAL	DRAWN		
FINISH	CHECKED		
	PROJ ENGRG/DSGN		
	MFG APPR		
	PROD ASSURANCE		
	PURCHASING		
	APPROVED		

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Systems Group
A Division of MEASUREMENT Systems & Controls
1601 Orangewood Ave / Orange, Calif. USA 92668 (714) 633-6440

TITLE HDC 2900

SIZE	DRAWING NO	REV
D	209402	A.1
SCALE	REV NO—FILE DATE	SHEET 3 OF 6

DWG. NO.	SH	REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

B8 COMMAND *
SH3-C5 SH5-D5
EQUAL *
SH3-C5

PAL16L8 U26
COMPARE 13
WRDATA * 4
RDATA * 2
BYTE * 6
DC2 9
SMA 7
SMAL 8
DC3 11
17 RAMCS *
18 RAMWE *
1 HALT *
14 T3
19
12
15 16

U17 LS04
13 12
1 2

RDLTC * A3
EQL B7

SMCNTLS
B7
SH1-C2,C3
SH2-D7
SH3-C8,D8
SH5-B2,B3,B5,C5,D3

P
D LS74 Q
C
U30
4 2 5 3 6 1

5VDC

SH2-B3 SH5-A3,C5 CLOCK
INIT * SH1-B1,B3,B5 SH3-C6 SH4-B6
CMDI * SH6-B7 SH1-B3,B4

LS273 U22
11 1 15
SH2-C4 SH3-B7 COMMAND * 14
C7 SMA 8
B6 RDATA3 7
NC 18
SH3-D5 RDATA2 13
C7 EQL 3
4
SH2-C4 SH3-B7 COMPLETE 17
9 SMAL B7
6 CPDATA C8
19 NC
12 RDATA3 B7
2
5
16

U21 LS240
8 12 1
2

U11 LS00
3 11 12

LS279 U29
5 10 1 6
R1 R3 R4 S1
S4 S2 S1
7 TIMEOUT SH2-D4 SH5-B7
4 DONE SH1-B5,C4
13 RTRY SH2-D6 SH5-B7
9 INTR SH2-B6,D6
Q1 Q4 Q2 Q3
R2
14
SH3-C6 CLRCRC

D4 TO *
SH5-B1 DNE * 2,3

SH5-D5 SH1-C4 SH2-D4 HALT
U21 LS240
13 7 HALT * D6

U11 LS00
10 9 8 TO * B6

SH3-A3 SH5-C5 INDX *
LS393 U18
12 13 8 11 2 3 1
NRZI SH2-D4
RA9

RAØ

LS393 U32
2 12 1 8 9 10 11 6 5 4 3 13
RA8 RA7 RA6 RA5 RA4 RA3 RA2 RA1

RAØ-4 RA8-9 SH5-D1

2114 U16
RA7 5
RA6 15
RA5 16
RA4 6
RA3 4
RA2 3
RAI 2
RAØ 1
17 RAH
7 RA8
8 RAMCS *
10 RAMWE *
14 DATA6
13 DATA4
12 DATA3
11 DATA1

2114 U25
RA7 5
RA6 15
RA5 16
RA4 6
RA3 4
RA2 3
RAI 2
RAØ 1
17 RAH
7 RA8
8 RAMCS *
10 RAMWE *
14 DATA7
13 DATA5
12 DATA2
11 DATAØ

DATAØ-7 SH1-A5 SH2-C8 SH3-C8 SH5-D1 SH6-C8

SH3-A5,C6 SH5-A5 CLOCK *
LS374 U24
11
DATA7 3
DATA6 18
DATA5 4
DATA4 17
DATA3 14
DATA2 7
DATAI 13
DATAØ 8
2 DATA7
19 DATA6
5 DATA5
16 DATA4
15 DATA3
6 DATA2
12 DATAI
9 DATAØ
C7 RDLTC *
1

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PROJ ENGR/DSGN		
MFG APPD		
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TITLE HDC 2900
SIZE D DRAWING NO 209402 REV A.1
SCALE REV BY—FILE DATE SHEET 4 OF 6

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A14700

DWG. NO.	SH	REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

LS375 U48 D Q G 9 10 12

PAL16L8 U33 16 SMAS2 8 SMAS3 7 Q1 1 Q2 4 Q3 2 SA 6 SB 11 Q4 17 13 RAH → SH4 D1 14 SI → SH3-D8 15 DCI → B3 18 HALT → SH1-C4 SH2-D4 SH4-D5 9 5 12

SMA*

SH1-A5 SH2-C8 SH4-C1 SH6-C8 DATAØ-3

SH3-C5 SH4-B8,D8 COMMAND* 9

LS163 U39 DATA3 6 DATA2 5 DATA1 4 DATAØ 3 CLOCK 2 ET 10 7 A2 A5 11 Q4 12 Q3 13 Q2 14 Q1 CCLR* 1 B5

Q4 11 U17 LS04 10 FORMAT* → SH6-B7

6309 U40 17 5 4 SMODE 19 SH1-C1 12 SMAS1 13 SMAS2 14 SMAS3

LS151 U34 B3 BYTE*7 SMA* 6 SMA 5 11 10 9 14 12 RDATA3 ← SH3-C7 13 SECTOR ← SH3-B2 15 E19 E18 1 RA4 2 RA2 3 RA1 4 RAØ RA9 RA8 RAØ-2,4,8-9 → SH4-D1

LS161 U47 2 6 7 10 1 3 4 5 15 5VDC SMA SH4-C7 INIT* SH1-B3,B5 12 13 14 1 3 2 4 5 15

U1 LS04 3 4 9

9 SA 11 SB 8 RGT 7 WGT 6 CP 3 18 4 7 8 15 16

LS377 U41 C5 DC1 13 SH3-C8 SH4-C7 DC2 14 12 SH4-C7 DC3 15 17 CLOCK 11 1 B5,D3 BYTE*

2 CSO → SH3-C6
19 CSI → SH3-A2
5 RGATE* → SH3-A2 SH6-B7
6 WRGATE* → SH3-A2 SH6-B7
9 COMPARE → SH4-D8
16 DNE* → SH4-B6

PAL16L8 U46 7 Q2 3 SH3-D1 DSØ 8 SH3-D1 SH6-D2 DSI 1 SH2-D6 SH4-B5 RTRY 5 SH2-D4 SH4-B6 TIMEOUT 2 SH1-C1 RUN 6 SH1-C1 CNTCLK 4 SH2-A6 Ø2* 9 19 CCLR* ← C5 11 14 DSA → SH3-B5 13 DSB → SH3-B5 16 ET → D5 17 DCLOCK → SH6-C2 15 12 18

B3 BYTE*

LS161 U27 7 5VDC 1 3 4 5 6 11 9 U17 LS04 8 12 T3 → SH4-D6 2 CLOCK → SH2-B3 SH4-B8 9 10

CLOCK

CLOCK

5 U17 LS04 6 CLOCK* → SH3-A5

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TITLE: HDC 2900

SIZE	DRAWING NO	REV
D	209402	A.1

SCALE — REV IN—FILE DATE — SHEET 5 of 6

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A14700

DWG. NO.	SH	REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

5VDC RP2 R220/330 SIP

P2

DATA7 17
DATA6 18
DATA5 15
DATA4 16
DATA3 13
DATA2 14
DATA1 11
DATAØ 12

LS640 U6

B A 19 1

ENABLL* → SH1-A6

SH1-A5 SH2-C8 SH3-C8 SH4-C1 SH5-D1 C6 DATAØ-7

ENABLL* 13
RDPB* 12
U11 LS00
11 2 18
U21 LS240

DIR* 11
STEP* 8
RDPB* 13
WRPB* 6
INIT* 15
RGATE* 4
WRGATE* 17
FORMAT* 2

S244 U5

SH3-C2 DIR*
SH3-C2 STEP*
SH1-B2 WRPB*
SH1-B5 SH5-B5 INIT*
SH3-A2 RGATE*
SH5-C1 SH3-A2 WRGATE*
SH5-C1 SH3-A2 FORMAT*
SH5-D3

1 19

C5 SH3-D1 DSI*

+16V SH2-B5

P2 pins: 16 15 14 13 12 11 10 9 | 22 24 26 28 30 40 42 48 60

5VDC

INDX* 16
RDY* 12
SECTOR* 3
TKO* 5
BDACK* 9
INT* 14
WRERR* 7
NC 18

LS244 U4

1 19

NC → NC

A8 SH3-D1 DSI*

SH2-D4,D6 SH3-B2

RP1 150Ω SIP

P2 pins: 44 32 46 38 20 36 34 | 3 8 17 21 23 25

SH3-A2 SH5-C1 WRDATA 2
3

9638 U12

8 7

P2 pins: 53 54 1 2

+8V SH2-C8

SH1-A3 PBCNT

MC3486 U13

SH3-D7 DRDATA 5
SH5-B7 DSI 4
SH5-A5 DCLOCK 3
12

100Ω R7 (6, 7)
100Ω R6 (2, 1)

P2 pins: 56 57 50 51

P2

PAØ 4
PA1 5
PA2 6
PA3 7
BSØ 18
BSI 19

P2 pins: 27 29 31 33 35 37 39 41 43 45 47 49 52 55 58

NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

APPROVAL	NAME	DATE
DRAWN		
CHECKED		
PROJ ENGR/DSGN		
QUAL APPD		
PROD ASSURANCE		
PURCHASING		
APPROVED		

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TITLE HDC 2900

SIZE D DRAWING NO 209402 REV A.1

SCALE REV IN—FILE DATE SHEET 6 OF 6

WARRANTY

All Products sold hereunder are warranted on a return-to-factory basis against defects in workmanship and material under normal and proper use for a period of one (1) year from the date of delivery.

As a condition of this warranty, purchaser must (i) obtain a Return Materials Authorization (RMA) Number and shipping instructions from Measurement Systems and Controls, Inc., (ii) ship the product, transportation prepaid, to the designated Measurement Systems and Controls, Inc. Repair Facility in the United States, and (iii) include with the returned product a written description of the claimed defect. Transportation charges for the return of the product to purchaser within the contiguous forty-eight (48) United States, Alaska, Hawaii and the District of Columbia will be paid by Measurement Systems and Controls, Inc. For products returned from all other locations, this warranty will be honored at the nearest Measurement Systems and Controls, Inc. Repair Facility in the United States but excludes all costs of transportation, customs clearance and any other related charges. If Measurement Systems and Controls, Inc. determines that the product is not defective as herein defined, purchaser shall pay Measurement Systems and Controls, Inc. all costs of handling and transportation and any repairs will be at the then prevailing Measurement Systems and Controls, Inc. repair rates.

Measurement Systems and Controls, Inc.'s sole responsibility under the above product warranties will be, at its option, to either repair or replace any component which fails during the period of the applicable warranty due to a defect in workmanship or material, provided purchaser has promptly reported same to Measurement Systems and Controls, Inc. All replaced products or parts shall become Measurement Systems and Controls, Inc.'s property.

All above warranties are contingent upon proper use of the product. These warranties will not apply (i) if adjustment, repair or parts replacement is required because of accident, unusual physical, electrical or electromagnetic stress, neglect, misuse, failure of electric power, air conditioning, humidity control, transportation, failure of rotating media not furnished by Measurement Systems and Controls, Inc., operation with media not meeting or not maintained in accordance with Measurement Systems and Controls, Inc. specifications or causes other than ordinary use, or (ii) if the product has been modified by purchaser, or (iii) where Measurement Systems and Controls, Inc. serial number or warranty date decals have been removed or altered, or (iv) if the product has been dismantled by purchaser without the supervision of or prior written approval of Measurement Systems and Controls, Inc.

EXCEPT FOR THE EXPRESS WARRANTIES CONTAINED HEREIN, MEASUREMENT SYSTEMS AND CONTROLS, INC. DISCLAIMS ALL WARRANTIES ON THE PRODUCTS FURNISHED HEREUNDER, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS; and the stated express warranties are in lieu of all obligations or liabilities on the part of Measurement Systems and Controls, Inc. arising out of or in connection with the performance of the products.

Measurement Systems and Controls, Inc. is not liable for any indirect or consequential damages.

After the warranty period, the products will be repaired for a service charge plus parts provided that it is returned prepaid to Measurement Systems and Controls, Inc. after retaining an RMA number.

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HDC-2900 Hard Disk Controller

1. Please specify by page any errors you found in this manual.

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2. Does the document cover the information you expected or required? Please make suggestions for improvement.

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3. Did you have any difficulty understanding descriptions or wording? Where?

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